Claims

[c1] 1. A driving circuit for a display, comprising:
a timing controller, used to receive a color driving signal, and to output a corresponding color driving signal according to a timing of the timing controller;
a data controller, having a multi-gray scale, wherein the data controller is coupled to the timing controller to receive the color driving signal, and to make the color driving signal correspond to a related gray of the multi-gray scale according to the multi-gray scale, so as to output a gray-level signal; and
an inverter, coupled to the data controller to receive the gray-level signal and to invert the gray-level signal, so as to output a color output signal to the display.

[c2] 2. The driving circuit for the display of claim 1, wherein the inverter inverts the gray-level signal according to a voltage level of the gray-level signal.

[c3] 3. The driving circuit for the display of claim 1, wherein the timing controller is further used to receive a clock signal (CLK), a horizontal synchronization signal (HSYNC), a vertical synchronization signal (VSYNC), and a differential enable signal (DE).

[c4] 4. The driving circuit for the display of claim 1, wherein the driving circuit is an ASIC (Application Specific Integrated

Circuit).

[c5] 5. The driving circuit for the display of claim 1, wherein the display is a LCD (Liquid Crystal Display).

[c6] 6. An operating method for a display driving circuit, comprising:
receiving a color driving signal, and outputting a corresponding color driving signal according to a timing;
receiving the color driving signal, and making the color driving signal correspond to a related gray of a multi-gray scale according to the multi-gray scale, so as to output a gray-level signal; and
inverting the gray-level signal, so as to output a color output signal to the display.

[c7] 7. The operating method for the display driving circuit of claim 6, wherein the multi-gray scale is included in a data controller in the driving circuit.

[c8] 8. The operating method for the display driving circuit of claim 6, wherein the gray-level signal is inverted by an inverter in the driving circuit.

[c9] 9. The operating method for the display driving circuit of claim 8, wherein the inverter inverts the gray-level signal according to a voltage level of the gray-level signal.

[c10] 10. The operating method for the display driving circuit of claim 6, wherein a timing controller in the driving circuit is used to receive the color driving circuit, and output the color driving circuit according to the timing.

[c11] 11. The operating method for the display driving circuit of claim 10, wherein the timing controller is further used to receive a clock signal (CLK), a horizontal synchronization signal (HSYNC), a vertical synchronization signal (VSYNC), and a differential enable signal (DE).

[c12] 12. The operating method for the display driving circuit of claim 6, wherein the driving circuit is an ASIC (Application Specific Integrated Circuit).

[c13] 13. The operating method for the display driving circuit of claim 6, wherein the display is an LCD (Liquid Crystal Display).